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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,870	BOHR ET AL.	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *17-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/01/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, claims **1 – 16** in the reply, filed on October 15, 2004, is acknowledged.

2. Claims **17 – 24** withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group II, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on October 15, 2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims **1, 2, 3, 8, 9** and **11** are rejected under 35 U.S.C. 102(e) as being anticipated by Noguchi et al. (US Patent No. 6,682,965).

5. Regarding claim **1**, Noguchi et al. disclose an apparatus comprising:

a substrate 11 (figs. 1 – 8B);

a device 2 (fig. 6) on the substrate including a gate electrode 13 (fig. 6) on a surface of the substrate and a first junction region 31 (fig. 6) and a second junction

region 32 (fig. 6) in the substrate adjacent the gate electrode; and a silicon alloy material 33 and 34 (fig. 6) disposed in each of the first junction region and the second junction region such that a surface of the first junction region and a surface of the second junction region are in a non-planar relationship with the surface of the substrate (column 6, lines 7 – 12).

Regarding claim **2**, Noguchi et al. disclose a surface of the substrate defines top surface of the substrate and the surface of the first junction region and the surface of the second junction region are superior to the top surface of the substrate (fig. 6).

Regarding claim **3**, Noguchi et al. disclose the surface of the first junction region and the surface of the second junction region are superior to the top surface of the substrate by a length in the range of between 5 nanometers and 150 nanometers (column 6, lines 10 – 12).

Regarding claim **8**, Noguchi et al. disclose a surface of the substrate proximate to the first junction region defines a first substrate sidewall surface and a surface of the substrate proximate to the second junction region defines a second substrate sidewall surface and the silicon alloy material disposed in the first junction region is attached to the first substrate sidewall surface and the silicon alloy material disposed in the second junction region is attached to the second substrate sidewall surface (see figure 6; side walls 17 and 18).

Regarding claim **9**, Noguchi et al. disclose the silicon alloy material comprises an epitaxial layer of silicon alloy material (column 6, lines 7 and 8).

Regarding claim **11**, Noguchi et al. disclose a layer of silicide material on the surface of the first junction region, the surface of the second junction region, and the gate electrode, wherein the layer of silicide material comprises titanium silicide (column 31 and 32).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims **4, 5, 6, 7, 14** and **15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi et al. (US Patent No. 6,682,965).

4. Regarding claim **4**, Noguchi et al. disclose claimed invention of claims 1 and 3, and the depth of the junction is 5 nm (column 5, lines 32 – 35). Noguchi does not explicitly show the first junction region and the second junction region define a depth in the range of between 30 nanometers and 250 nanometers in depth.

However, it would have been well known in the art that the selection of those parameters such as **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.**, would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.**, or in conbination of the parameters would be an unpatentable modification. Under some circumstances, however, changes such as these may impart

patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

Moreover, the depth has not been alleged by applicant to be of significant importance for patentability.

Regarding claims **5, 6** and **7**, Noguchi et al. disclose claimed invention of claim 1, except for the substrate is under a strain caused by a silicon alloy lattice spacing of the silicon alloy (cited in claim 5); the silicon alloy material has a silicon alloy lattice spacing that is different than a lattice spacing of the substrate material (cited in claim 6); and the substrate is under a strain caused by a silicon alloy lattice spacing being a larger lattice spacing than the lattice spacing of the substrate material.

However, Noguchi et al. show the device structure similar to the claimed structure. Therefore, it is fair to say that, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to recognize Noguchi's device would have a substrate being under a strain caused by a silicon alloy lattice spacing of

the silicon alloy; the silicon alloy material has a silicon alloy lattice spacing that is different than a lattice spacing of the substrate material; and the substrate is under a strain caused by a silicon alloy lattice spacing being a larger lattice spacing than the lattice spacing of the substrate material.

Regarding claim **14**, Noguchi et al. disclose 14. An apparatus comprising:

a substrate 11 (figs. 1 – 8B);

a device 2 (fig. 6) on the substrate including a gate electrode 13 (fig. 6) on a surface of the substrate and a first junction region 31 (fig. 6) and a second junction region 32 (fig. 6) in the substrate adjacent the gate electrode; and a silicon alloy material 33 and 34 (fig. 6) disposed in each of the first junction region and the second junction region such that a surface of the first junction region and a surface of the second junction region are superior to the top surface of the substrate by a length sufficient to cause a strain in the substrate (column 6, lines 7 – 12).

Noguchi et al. do not explicitly teach the silicon alloy material having a silicon alloy lattice spacing that is different than a lattice spacing of the substrate.

However, Noguchi et al. show the device structure similar to the claimed structure. Therefore, it is fair to say that, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to recognize Noguchi's device would have a silicon alloy material having a silicon alloy lattice spacing that is different than a lattice spacing of the substrate.

Regarding claim **15**, Noguchi et al. disclose the substrate comprises an N-type channel/well material of one of silicon, polycrystalline silicon, and single crystal silicon

having an electrically negative charge, and wherein the silicon alloy material comprises a P-type junction region material having an electrically positive charge (column 2, lines 25+ and column 3, lines 3+).

8. Claims **10, 12, 13** and **16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi et al. (US Patent No. 6,682,965) in view of Murthy et al. (US Patent No. 6,214,679 (IDS)).

Regarding claim **10**, Noguchi et al. disclose the claimed invention of claim 1 except for the silicon alloy material comprises

one of silicon germanium (Si_{y-x} Ge_x), silicon carbide (Si_{y-x} C_x), nickel silicide (NiSi), titanium silicide (TiSiz), and cobalt silicide (CoSiz).

Murthy et al. show recesses 218 are filled with silicon germanium (Si_x GE_{100-x}) alloy (column 5, lines 41 – 42).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the silicon alloy of Noguchi with the silicon germanium of Murthy, in order to take advantage of being capable of controlling the lattice constant of their mixture by changing their mixture ratio to form crystals from the mixture of silicon and germanium.

Regarding claims **12** and **13**, Murthy et al. disclose a layer 224 (not shown) made of silicon nitride (column 6, line 58 and 59) on the layer of silicide material (note: silicon nitride layer 224 can be used as an etch stop layer and as a dielectric layer as needed).

Regarding claim **16**, Noguchi et al. disclose the claimed invention of claim 14 except for the silicon alloy is silicon germanium having a lattice spacing that is larger

than a lattice spacing of the N-type channel/well material, and wherein the strain is a compressive strain.

Murthy et al. show recesses 218 are filled with silicon germanium ($Si_x GE_{100-x}$) alloy (column 5, lines 41 – 42).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the silicon alloy of Noguchi with the silicon germanium of Murthy, in order to take advantage of being capable of controlling the lattice constant of their mixture by changing their mixture ratio to form crystals from the mixture of silicon and germanium.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Tran

November 23, 2004

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